ABSTRACT OF THE DISCLOSURE

An output buffer circuit of the present invention includes a plurality of unit circuits in each of which a pull-up transistor controlled by a first input signal is connected between a high-potential power supply and common node, and a pull-down transistor controlled by a second input signal is connected between the common node and a low-potential power supply, an output terminal connected to a common connecting point of the common nodes of the plurality of unit circuits, and first resistors formed respectively between the common nodes of the plurality of unit circuits and the common connecting point.